

Customer No.: 31561  
Docket No.: 13292-US-PA  
Application No.: 10/709,767

### AMENDMENTS

#### In The Claims

1. (currently amended) A printhead controller implemented within a printhead, wherein said printhead is one of a plurality of printheads in a printer, comprising:

a circuit, for receiving an address signal and a selection signal, said selection signal being one of a plurality of selection signals provided by a printhead selection circuit of a printhead drive unit in said printer to selectively enable said printhead, said circuit including a plurality of inverters connected in series, said plurality of inverters including at least a first inverter and a second inverter, said first inverter receiving said selection signal, each of said plurality of inverters of said circuit receiving the same said address signal, and said second inverter outputting a switching signal corresponding to said selection signal and said address signal; and

an ink jetting circuit, for receiving said switching signal from said circuit and determining whether or not to jet out ink based on said switching signal, and

wherein said address signal and said selection signal have a voltage level of a logic high voltage level and a logic low voltage level, said switching signal is a logic high voltage level and selectively enables said ink jetting circuit when said address signal and said selection signal are at the logic high voltage level.

2. (previously presented) The printhead controller of claim 1, wherein said address signal is a working driving voltage of said circuit.

3. (canceled)

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4. (previously presented) The printhead controller of claim 1, wherein each of said inverters includes a FET.

5. (currently amended ) ~~The printhead controller of claim 4~~ A printhead controller implemented within a printhead, comprising:

a circuit, for receiving an address signal and a selection signal, said circuit including a plurality of inverters connected in series, and outputting a switching signal corresponding to said selection signal and said address signal; and

an ink jetting circuit, for receiving said switching signal and determining whether or not to jet out ink based on said switching signal,

wherein each of said inverters includes a FET,

wherein said circuit includes:

a first resistor, having a first terminal for receiving said address signal;

a first FET, having a first terminal being coupled to a second terminal of said first resistor and outputting an inverted signal, a second terminal for receiving said selection signal, and a third terminal being coupled to a ground;

a second resistor, having a first terminal for receiving said address signal; and

a second FET, having a first terminal being coupled to a second terminal of said second resistor and outputting said switching signal, a second terminal for receiving said inverted signal, and a third terminal being coupled to said ground.

6. (original) The printhead controller of claim 5, wherein a resistance of said first resistor and said second resistor range from 0.5k $\Omega$  to 500k $\Omega$ .

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7. (original) The printhead controller of claim 5, wherein a resistance of said first resistor and said second resistor range from 20k $\Omega$  to 80k $\Omega$ .

8. (withdrawn) The printhead controller of claim 4, wherein said buffer circuit includes:  
a first FET, having a first terminal for receiving said address signal, a second terminal coupled to said first terminal of said first FET, and a third terminal for outputting an inverted signal;

a second FET, having a first terminal being coupled to said third terminal of said first FET, and a second terminal for receiving said selection signal;

a third FET, having a first terminal being coupled to a third terminal of said second FET, a second terminal for receiving a second selection signal, and a third terminal being coupled to a ground;

a fourth FET, having a first terminal for receiving said address signal, a second terminal being coupled to said first terminal of said fourth FET, and a third terminal for outputting said buffer signal; and

a fifth FET, having a first terminal being coupled to said third terminal of said fourth FET, a second terminal for receiving said inverted signal, and a third signal being coupled to said ground.

9. (withdrawn) The printhead controller of claim 8, wherein said first FET is replaced by a first resistor, and said first resistor has a first terminal for receiving said address signal and a second terminal being coupled to said first terminal of said second FET.

10. (withdrawn) The printhead controller of claim 8, wherein said second selection signal is said address signal.

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11. (withdrawn) The printhead controller of claim 4, wherein said buffer circuit includes:
- a first resistor, having a first terminal for receiving said address signal;
  - a first FET, having a first terminal being coupled to a second terminal of said first resistor and outputting an inverted signal, a second terminal for receiving said selection signal, and a third terminal being coupled to a ground;
  - a second FET, having a first terminal for receiving said address signal, a second terminal being coupled to said first terminal of said second FET, and a third terminal for outputting said buffer signal; and
  - a third FET, having a first terminal being coupled to said third terminal of said second FET, a second terminal for receiving said inverted signal, and a third terminal being coupled to said ground.
12. (withdrawn) The printhead controller of claim 11, wherein a resistance of said first resistor ranges from 0.5k $\Omega$  to 500k $\Omega$ .
13. (withdrawn) The printhead controller of claim 11, wherein a resistance of said first resistor ranges from 20k $\Omega$  to 80k $\Omega$ .
14. (withdrawn) The printhead controller of claim 4, wherein said buffer circuit includes:
- a first resistor, having a first terminal for receiving said address signal;
  - a first FET, having a first terminal being coupled to a second terminal of said first resistor and outputting an inverted signal, a second terminal for receiving said selection signal, and a third terminal being coupled to a ground;
  - a second FET, having a first terminal for receiving said address signal, and a third terminal for outputting said buffer signal;

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a third FET, having a first terminal being coupled to said first terminal and a second terminal of said second FET, a second terminal and a third terminal being coupled to said third terminal of said second FET; and

a fourth FET, having a first terminal being coupled to said third terminal of said second FET, a second terminal for receiving said inverted signal, and a third terminal being coupled to said ground.

15. (withdrawn) The printhead controller of claim 14, wherein a resistance of said first resistor ranges from  $0.5\text{k}\Omega$  to  $500\text{k}\Omega$ .

16. (withdrawn) The printhead controller of claim 14, wherein a resistance of said first resistor ranges from  $20\text{k}\Omega$  to  $80\text{k}\Omega$ .

17-20. (cancelled)